REMARKS

Claims 1, 3-24, and 29-33 remain in this application. Claims 1, 5-6, 9, 13, 15-19, 22, 29, and 31-33 have been amended. The limitations relied upon to distinguish over the cited art have not been altered, therefore the Applicants respectfully submit that the amendments do not raise new issues for purposes of examination. The amended claims are supported by the specification. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

Specification

The Applicants propose herein amendments to the specification to correct informalities. It is respectfully submitted that no new matter has been introduced by these amendments. In particular, the logic device 25 is shown in Figures 3, 4, and 5.

35 U.S.C. §103(a) Rejection - Gates

The Examiner has rejected claims 1, 4-6, 9-24, and 29-33 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,701,409 issued to Gates (hereinafter referred to as "Gates") in view of allegedly well-known art. In particular, the Examiner has provided U.S. Patent Number 5,086,500 to Greub (hereinafter referred to as "Greub") to support the assertion that multiple commands may be stored in an instruction memory for the purpose of speeding up the time needed to process instructions.

The Rejection of Claim 1 is Overcome

The last Office Action rejected independent claim 1 on Gates. Applicants request reconsideration of this rejection because even if the assertion that storing multiple instructions in an instruction memory is well known, which it may not be, Gates in view of such an assertion still does not teach a **predefined sequence of instructions**.

Claim 1 recites, "one or more phase generators to drive a series of signals on the bus corresponding to the predefined **bus stimuli instructions in a predefined sequence**". Applicants provide the following discussion from the specification to illustrate, without limitation, the uses and advantages of a predefined sequence of instructions, according to one exemplary embodiment (page 7, lines 5-12):

> "Components ... often contain bugs that cause them to fail during operation. In the failing scenarios, the components frequently respond incorrectly to specific bus transaction sequences, even when the bus transaction sequence is "legal"; in other words, there is nothing in the bus transaction sequence that should have caused the component to fail. The process of correcting these bugs requires inducing the failure under controlled conditions to isolate the bug. Part of this process may require repeating the bus transaction sequence corresponding to the failure."

Advantageously, in this particular example, a legal sequence of bus stimuli instructions may be used to detect bugs in components coupled with the bus that incorrectly perceive the legal sequence as an error. Other exemplary uses are contemplated.

In contrast, Gates does not teach or suggest a predefined sequence of instructions. As understood by the Applicants, Gates discusses a bus error generation circuit that "generates an error condition on the bus" (abstract) as a result of executing a **single**

command. This is done by loading a **single** error command (e.g., the commands shown in Figures 7 and 9A-9H) into a register of the circuit, then the circuit decoding the single command, and then the circuit generating a corresponding error condition onto the PCI bus. As understood by the Applicants, the Figures 2, 4, and 9A-H each refer to multiple phases within a single command. By way of example, Figure 4 shows multiple phases within a **single** write command and in particular shows incorrect parity control circuit 110 controlling gate 109 "to output the incorrect parity value onto parity bus terminal 106" (column 4, lines 40-41) during a particular phase. Thus, the errors in Gates refer only to a single command. Accordingly, and without limiting the present invention to the exemplary use mentioned above, **Gates may be used to test whether bus components detect and respond to an error for a single command but cannot test whether components respond correctly to predefined sequences of multiple bus stimuli instructions.**

Greub also does not teach or suggest a predefined sequence of bus stimuli instructions. Thus, a predefined sequence of bus stimuli instructions is clearly foreign to the cited art. Accordingly, claim 1 is believed to be allowable.

Claims 3-14 and 32-33 depend from claim 1 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

The Rejections of Independent Claims 15, 21, 29 and 31 Are Similarly Overcome

Claim 15 recites, "an instruction memory to store a predefined sequence of bus stimuli". Accordingly, claim 15 is believed to be allowable for reasons similar to those discussed for claim 1.

Claim 21 recites, "receiving instruction words corresponding to predefined bus stimuli,

the predefined bus stimuli representing a plurality of bus transactions". Accordingly, claim 21 is believed to be allowable for reasons similar to those discussed for claim 1. Claims 22-24 depend from claim 21 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 29 recites, "predefined bus stimuli instructions representing signals associated with a plurality of bus transactions on a bus". Accordingly, claim 29 is believed to be allowable for reasons similar to those discussed for claim 1. Claim 30 depends from claim 29 and is believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 31 recites, "generating a plurality of instruction words corresponding to a predefined sequence of bus transactions". Accordingly, claim 31 is believed to be allowable for reasons similar to those discussed for claim 1.

The Rejection of Claim 16 is Overcome

The last Office Action rejected independent claim 16 on Gates. Claim 16 recites, "second means to drive the plurality of predefined bus transactions as signals on the bus". Applicants request reconsideration of this rejection because Gates does not teach or suggest the **specific structures** described in the application, corresponding to the "second means".

Accordingly, claim 16 is believed to be allowable. Claims 17-20 depend from claim 16 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Official Notice

The Examiner has taken Official Notice that instruction words of predefined lengths are well known in the art. The Applicants respectfully submit that the use of instruction words having a predefined length in the system of claim 6 is not well known. If the Examiner persists in this rejection, it is respectfully requested that a reference be provided in support of this submission.

The Examiner has taken Official Notice that FPGAs and ASICs are well known in the art. The Applicants respectfully submit that using FPGAs and ASICs in the system of claim 6 is not well known. If the Examiner persists in this rejection, it is respectfully requested that a reference be provided in support of this submission.

The Dependent Claims Are Even More Distinguishable Over Cited Art

Claim 22 recites, "defining a sequence of desired bus transactions" and "assembling the sequence of desired bus transactions into instruction words". Gates does not teach or suggest these limitations. Accordingly, claim 22 is believed to be allowable.

Claim 32 recites, "an interface other than the bus coupled with the instruction memory, the interface to connect with a device to receive a plurality of predefined bus stimuli instructions". Gates does not teach or suggest this limitation. Accordingly, claim 32 is believed to be allowable.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Date: May 29,2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

The paragraph beginning at page 12, line 16 has been amended as follows:

Fig. 5 is a block diagram illustrating a particular embodiment of a transaction generator 20 in accordance with the present invention. The embodiment of Fig. 5 implements the transaction generator 20 with an Intel® Pentium® Pro processor bus. While Fig. 5 illustrates an implementation of the transaction generator 20 with the Pentium® Pro processor bus, the present invention is not limited to any particular type of bus. It would be well within the ordinary skill in the art to apply the present invention to other bus types by one in the art having the benefit of this disclosure. In the exemplary embodiment of Fig. 5, [the phase generator 24] the logic device 25 comprises three field programmable gate arrays (FPGA) 50,.52, 54. Suitable FPGA's, for example, include model 4036XL or 4062XL FPGAs available from Xilinx® Inc., San Jose, CA. The FPGAs 50, 52, 54 may be programmed using a hardware descriptive language as is known in the art, such as VHDL or Verilog. Alternately, application specific integrated circuits (ASIC) may be designed, or discrete logic devices may be arranged, to implement the digital logic functions of the transaction generator 20 by one skilled in the art having the benefit of this disclosure.

In The Claims:

1. (Amended) A system comprising:

[Instruction] an instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing a plurality of bus transactions; and

[One] one or more phase generators coupled [between] with a bus and the instruction memory, the one or more phase generators to drive a series of signals on the bus corresponding to the predefined bus stimuli instructions in a predefined sequence.

5. (Amended) The system of claim 1, further comprising a response memory coupled [to] with the phase generator [storing] to store predefined responses to signals received from the bus.

6. (Amended) The system of claim 1, wherein the at least one of the one or more phase generators includes at least one digital logic device responsive to the instructions and at least one phase engine [for controlling] to control timing of the bus stimuli.

9. (Amended) The system of claim 6, wherein the at least one digital logic device includes a control portion [for providing] to provide bus control signals and a data portion [for sending] to send data to the bus.

13. (Amended) The system of claim 9, further comprising a data memory coupled [to] with the data portion.

15. (Amended) A system comprising:

an instruction memory [for storing] to store a predefined sequence of bus stimuli representing a plurality of bus transactions;

a flow logic device responsive to the instruction memory;

a request logic device responsive to the instruction memory;

a data logic device responsive to the instruction memory;

a data memory coupled [to] with the data logic device [for storing] to store data to be exchanged with agents on a bus;

a system protocol generator coupled [to] with the bus and the flow logic device;

an arbitration protocol generator coupled [to] with the flow logic device and the bus;

a request protocol generator coupled [to] with the flow logic device, the request logic device and the bus;

a snoop/error protocol generator coupled [to] with the request logic device and the bus;

a data protocol engine coupled [to] with the data logic device; and

a transaction response memory coupled [to] with the flow logic device and the request logic device to store [storing] digital data representing predefined responses to signals received from the bus.

16. (Amended) A system comprising:

a first means to store [for storing] instructions representing a plurality of predefined bus transactions; and

second means to drive [for driving] the plurality of predefined bus transactions as signals on the bus.

17. (Amended) The system of claim 16, further comprising third means [for storing] to store data representing predefined responses to signals received from the bus, and wherein the second means implements the predefined responses based on the signals received from the bus.

18. (Amended) The system of claim 16, further comprising fourth means [for controlling] to control the timing of the signals provided to the bus by the second means.

19. (Amended) The system of claim 16, further comprising fifth means [for storing] to store data to be exchanged with agents on the bus, wherein the second means transmits data from the fifth means in response to the instructions stored in the first means.

22. (Amended) The method of claim 21, further comprising [the acts of]:

defining a sequence of desired bus transactions; and

assembling the sequence of desired bus transactions into instruction words wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus.

29. (Amended) A system comprising:

an instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing signals associated with a plurality of bus transactions on a bus;

at least one phase generator coupled [between] with the bus and the instruction memory, the at least one phase generator to provide signals to the bus corresponding to the predefined bus stimuli instructions.

31. (Amended) A method comprising:

generating a plurality of instruction words corresponding to a predefined sequence of bus transactions;

storing the instruction words in a memory; and

executing the bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence.

32. (Amended) The system of claim 1, further comprising:

an interface other than the bus coupled [to] with the instruction memory, the interface [for connection] to connect with a device to receive a plurality of predefined bus stimuli instructions.

33. (Amended) The system of claim 1, wherein the plurality of predefined bus stimuli instructions are [configured as] to drive a predefined ordered sequence of bus transactions onto the bus.